EE8351 DIGITAL LOGIC CIRCUITS

UNIT-I NUMBERING SYSTEMS AND DIGITAL LOGIC FAMILIES

1) What are basic properties of Boolean algebra?

The basic properties of Boolean algebra are commutative property, associative Property and distributive property.

2) State the associative property of boolean algebra.

The associative property of Boolean algebra states that the OR ing of several variables results in the same regardless of the grouping of the variables. The associative property is stated as follows: A+ (B+C) = (A+B) +C

3) State the commutative property of Boolean algebra.

The commutative property states that the order in which the variables are OR ed makes no difference. The commutative property is: A+B=B+A

4) State the distributive property of Boolean algebra.

The distributive property states that AND ing several variables and OR ing the result With a single variable is equivalent to OR ing the single variable with each of the the several Variables and then AND ing the sums. The distributive property is: A+BC= (A+B) (A+C)

5) State the absorption law of Boolean algebra.

The absorption law of Boolean algebra is given by X+XY=X, X(X+Y) =X.

6) State De Morgan's theorem.

De Morgan suggested two theorems that form important part of Boolean algebra. They are,

1) The complement of a product is equal to the sum of the complements. (AB)' = A' + B'

2) The complement of a sum term is equal to the product of the complements. (A + B)' = A'B'

7) Reduce A (A + B)

A (A + B) = AA + AB= A (1 + B) [1 + B = 1]= A.

8) Reduce A'B'C' + A'BC' + A'BC

A'B'C' + A'BC' + A'BC = A'C'(B' + B) + A'B'C

= A'C' + A'BC [A + A' = 1]

= A'(C' + BC)

= A'(C' + B) [A + A'B = A + B]

9) Simplify the following expression Y = (A + B) (A + C') (B' + C')

Y = (A + B) (A + C') (B' + C')

= (AA' + AC +A'B +BC) (B' + C') [A.A' = 0]

= (AC + A'B + BC) (B' + C')

= AB'C + ACC' + A'BB' + A'BC' + BB'C + BCC'

= AB'C + A'BC'

10) Show that (X + Y' + XY) (X + Y') (X'Y) = 0

(X + Y' + XY)(X + Y')(X'Y) = (X + Y' + X) (X + Y') (X' + Y) [A + A'B = A + B]

= (X + Y') (X + Y') (X'Y) [A + A = 1]

= (X + Y') (X'Y) [A.A = 1]

= X.X' + Y'.X'.Y

= 0 [A.A' = 0]

12) Prove that ABC + ABC' + AB'C + A'BC = AB + AC + BC

ABC + ABC' + AB'C + A'BC=AB(C + C') + AB'C +
A'BC =AB + AB'C + A'BC
=A(B + B'C) +
A'BC =A(B + C) +
A'BC =AB + AC +
A'BC =B(A + C) +
AC =AB + BC + AC
=AB + AC +BC ...Proved

13) Convert the given expression in canonical SOP form Y = AC + AB + BC

Y = AC + AB + BC

=AC (B + B') + AB (C + C') + (A + A') BC

=ABC + ABC' + AB'C + AB'C' + ABC + ABC' + ABC
=ABC + ABC' +AB'C + AB'C' [A + A =1]

14) Define duality property.

Duality property states that every algebraic expression deducible from the postulates Of Boolean algebra remains valid if the operators and identity elements are interchanged. If the dual of an algebraic expression is desired, we simply interchange OR and AND operators and replace 1's by 0's and 0's by 1's.

15) Find the complement of the functions F1 = x'yz' + x'y'z and F2 = x (y'z' + yz). By applying De-Morgan's theorem.

F1' = (x'yz' + x'y'z)' = (x'yz')'(x'y'z)' = (x + y' + z)(x + y +z')

F2' = [x (y'z' + yz)]' = x' + (y'z' + yz)'

= x' + (y'z')'(yz)'

= x' + (y + z) (y' + z')

16) Simplify the following expression
Y = (A + B) (A = C) (B + C)

= (A A + A C + A B + B C) (B + C)

= (A C + A B + B C) (B + C)

= A B C + A C C + A B B + A B C + B B C + B C C = A B C

17) What are the methods adopted to reduce Boolean function?

i) Karnaug map ii) Tabular method or Quine Mc-Cluskey method

iii) Variable entered map technique.

18) State the limitations of karnaugh map.

i) Generally it is limited to six variable map (i.e) more then six variable involving expression are not reduced.

ii) The map method is restricted in its capability since they are useful for simplifying only Boolean expression represented in standard form.

19) What is a karnaugh map?

A karnaugh map or k map is a pictorial form of truth table, in which the map diagram is made up of squares, with each squares representing one minterm of the function.44) Find the minterms of the logical expression

Y = A'B'C' + A'B'C + A'BC + ABC'

Y = A'B'C' + A'B'C + A'BC + ABC'

=m0 + m1 +m3 +m6

=_m (0, 1, 3, 6)

20) Write the maxterms corresponding to the logical expression Y = (A + B + C') (A + B' + C') (A' + B' + C)

= (A + B + C') (A + B' + C') (A' + B' + C)

=M1.M3.M6

= M (1, 3, 6)

PART-B

1. Write notes on digital logic families?**(9 Mark)[April/May 2011]**
2. Compare the characteristics of TTL, ECL and CMOS logic families?**(16 Mark)[April/May 14][OR]**
3. Draw the circuit diagram and explain the operation of 2 input TTL NAND gate with open collector output **(16 Mark)[Nov/Dec 11] [OR]**
    - Explain in detail about TTL with open Collector output configuration? **(8 Mark)[Nov/Dec 2013][Nov/Dec 2010]**
4. With circuit schematic explain the operation of a two input TTL NAND gate**. (8) (MAY 2016& 17)**
5. Design a TTL circuit 3 input NAND gate (8) **(Nov/Dec 2014)**
6. With circuit schematic, explain the operation of a two input TTL NAND gate with totem pole output **(10) (May/June 2015)**
7. Compare totem pole and open collector outputs**(6) (May/June 2015),(MAY 17)**
8. With circuit schematic and explain the operation and characteristics of a ECL gate**. (8) (MAY 2016)**
9. Demonstrate the CMOS logic circuit configuration and characteristics in detail?**(8 Mark)[Nov/Dec 2013][Nov/Dec 2010]**
10. Draw the CMOS logic circuit for NOR gate and explain its operation(8) **(NOV/DEC 2015)**
11. Explain with an aid of circuit diagram the operation of 2 input CMOS NAND gate and list out its advantages over other logic families.(10) **(NOV/DEC 2016)**
12. Compare all the IC logic families based on:
    (i) Power Consumption
    (ii) Fan out
    (iii) Power Dissipation
    (iv) Propagation Delay
    (v) Switching Speed

UNIT-II

COMBINATIONAL CIRCUITS

1) What are called don't care conditions?

In some logic circuits certain input conditions never occur, therefore the Corresponding output never appears. In such cases the output level is not defined, it can be either high or low.

These output levels are indicated by 'X' or'd' in the truth tables and are called don't care conditions or incompletely specified functions.

2) What is a prime implicant?

A prime implicant is a product term obtained by combining the maximum possible number of adjacent squares in the map.

3) What is an essential implicant?

If a min term is covered by only one prime implicant, the prime implicant is said to be Essential.

4) Define combinational logic.

When logic gates are connected together to produce a specified output for certain specified combinations of input variables, with no storage involved, the resulting circuit is called combinational logic.

5) Write the design procedure for combinational circuits. x The problem definition

- x Determine the number of available input variables & required O/P variables.
- x Assigning letter symbols to I/O variables
- x Obtain simplified Boolean expression for each O/P.
- x Obtain the logic diagram.

6) Define half adder and full adder.

The logic circuit that performs the addition of two bits is a half adder. The circuit that Performs the addition of three bits is a full adder.

7) Define Decoder.

A decoder is a multiple - input multiple output logic circuit that converts coded inputs into coded outputs where the input and output codes are different.

8) What is binary decoder?

A decoder is a combinational circuit that converts binary information from n input lines to a maximum of 2n out puts lines.

9) Define Encoder.

An encoder has 2n input lines and n output lines. In encoder the output lines generate the binary code corresponding to the input value.

10) What is priority Encoder?

A priority encoder is an encoder circuit that includes the priority function. In priority encoder, if 2 or more inputs are equal to 1 at the same time, the input having the highest priority will take precedence.

12) Define multiplexer.

Multiplexer is a digital switch. If allows digital information from several sources to be routed onto a single output line.

13) What do you mean by comparator?

A comparator is a special combinational circuit designed primarily to compare the relative magnitude of two binary numbers.

14) Write down the steps in implementing a Boolean function with levels of NAND Gates. x Simplify the function and express it in sum of products.

- x Draw a NAND gate for each product term of the expression that has at least two Literals.

- This constitutes a group of first level gates.
- Draw a single gate using the AND-invert or the invert- OR graphic symbol in the second level, with inputs coming from outputs of first level gates.
- A term with a single literal requires an inverter in the first level. How ever if the single literal is complemented, it can be connected directly to an input of the second level NAND gate.

15) Give the general procedure for converting a Boolean expression in to multilevel NAND diagram?

- Draw the AND-OR diagram of the Boolean expression.
- Convert all AND gates to NAND gates with AND-invert graphic symbols.
- Convert all OR gates to NAND gates with invert-OR graphic symbols.
- Check all the bubbles in the same diagram. For every bubble that is not compensated by another circle along the same line, insert an inverter or complement the input literal.

PART-B

1. Design a 4-bit BCD to excess 3 code convertor and implement using logic gates**(8)(NOV/DEC 2015)**
   - Design BCD to Excess-3 code converter **(8) (APRIL/MAY 2015) [Nov/Dec 2013] (MAY/JUNE 2016)**
   - Design a logic circuit to convert the 8421 BCD to Excess 3 code**.[12 Mark][Apr/May 2010**
2. Design a Full adder using two Half adders and an OR gate **(8) (APRIL/MAY 2015)**
   - Implement Full Adder using two Half Adders? **[8 Mark]**
3. Design a full subtractor and implement using logic gates**(8) (NOV/DEC 2015) (Nov/Dec 2014)**
4. Design and implement a Binary to Gray code converter? **[16 Mark] [OR]**
   - Design and implement a 8421 to Gray code converter. Realize the converter using only NAND gates.[16 Mark] [May/June 2009]
   - Design a 4-bit Binary to gray code converter and implement it using logic gates.(8) (Nov/Dec 2014)
5. Simplify using K-map F(A,B,C,D) = $\sum m(7,8,9) + d(10,11,12,13,14,15)$**[8 Mark][Nov/Dec 2013]**
6. Simplify the Boolean Function using K-map F(w,x,y,z) = Σ(1,3,7,11,15) which has the don't care conditions d(w,x,y,z)= $\sum(0,2,5)$? **[16 Mark][May/June 2013]**
7. Reduce the following function using K-map f(*A,B,C,D*)=$\prod M(0,2,3,8,9,12,13,15)$ **(APRIL 2015)**
8. Simplify the logical expression using K-map in SOP and POS form. F(A,B,C,D)=Σm(0,2,3,6,7)+d(8,10,11,15)**(13) (NOV/DEC 2016)**

9. Solve $g(w,x,y,z) = \sum m(1,3,4,6,11) + d(0,8,10,12,13)$ **[8 Mark] [Apr/May 2010]**

10. Implement the given function using Multiplexer **f(w,x,y,z)=Σm(0,1,3,5,6,7,8,12,14)+Σd(9,15) [6 Mark] [May 2017]**
11. Design a full adder using only NOR gates.**(6) [MAY 2017]**

UNIT-III

SYNCHRONOUS SEQUENTIAL CIRCUITS

1. What are the classifications of sequential circuits?

The sequential circuits are classified on the basis of timing of their signals into two types.

They are, 1) Synchronous sequential circuit. 2) Asynchronous sequential circuit.

2. Define Flip flop.

The basic unit for storage is flip flop. A flip-flop maintains its output state either at 1 or 0 until directed by an input signal to change its state.

3. What are the different types of flip-flop?

There are various types of flip flops. Some of them are mentioned below they are,

(1) RS flip-flop (2) SR flip-flop (3) D flip-flop

(4) JK flip-flop (5) T flip-flop

4. What is the operation of RS flip-flop?

x When R input is low and S input is high the Q output of flip-flop is set. x
When R input is high and S input is low the Q output of flip-flop is reset. x
When both the inputs R and S are low the output does not change

x When both the inputs R and S are high the output is unpredictable.

5. What is the operation of SR flip-flop?

- When R input is low and S input is high the Q output of flip-flop is set.
- When R input is high and S input is low the Q output of flip-flop is reset.
- When both the inputs R and S are low the output does not change.
- When both the inputs R and S are high the output is unpredictable.

6. What is the operation of D flip-flop?

In D flip-flop during the occurrence of clock pulse if D=1, the output Q is set and if D=0, the output is reset.

7. What is the operation of JK flip-flop?

x When K input is low and J input is high the Q output of flip-flop is set. x
When K input is high and J input is low the Q output of flip-flop is reset. x
When both the inputs K and J are low the output does not change

x When both the inputs K and J are high it is possible to set or reset the Flip-flop (ie) the output toggle on the next positive clock edge.

8. What is the operation of T flip-flop?

T flip-flop is also known as Toggle flip-flop.

x When T=0 there is no change in the output.

x When T=1 the output switch to the complement state (ie) the output toggles.

9. Define race around condition.

In JK flip-flop output is fed back to the input. Therefore change in the output results change in the input. Due to this in the positive half of the clock pulse if both J and K are high then output toggles continuously. This condition is called race around condition'.

10. What is edge-triggered flip-flop?

The problem of race around condition can solved by edge triggering flip flop. The term edge triggering means that the flip-flop changes state either at the positive edge or negative edge of the clock pulse and it is sensitive to its inputs only at this transition of the clock.

11. What is a master-slave flip-flop?

A master-slave flip-flop consists of two flip-flops where one circuit serves as a master and the other as a slave.

12. Explain the flip-flop excitation tables for RS FF.

In RS flip-flop there are four possible transitions from the present state to the next state. They are,

x _ 0_0 transition: This can happen either when R=S=0 or when R=1 and S=0.

x _ 0_1 transition: This can happen only when S=1 and R=0.

x _ 1_0 transition: This can happen only when S=0 and R=1.

x _ 1_1 transition: This can happen either when S=1 and R=0 or S=0 and R=0.

13. Explain the flip-flop excitation tables for JK flip-flop

In JK flip-flop also there are four possible transitions from present state to next state. They are,

x _ 0_0 transition: This can happen when J=0 and K=1 or K=0.

x _ 0_1 transition: This can happen either when J=1 and K=0 or when J=K=1.

x _ 1_0 transition: This can happen either when J=0 and K=1 or when J=K=1.

x _ 1_1 transition: This can happen when K=0 and J=0 or J=1.

14. Explain the flip-flop excitation tables for D flip-flop

In D flip-flop the next state is always equal to the D input and it is independent of the present state.

Therefore D must be 0 if Qn+1 has to 0, and if Qn+1 has to be 1 regardless the value of Qn.

15. Explain the flip-flop excitation tables for T flip-flop

When input T=1 the state of the flip-flop is complemented; when T=0, the state of the Flip-flop remains unchanged. Therefore, for 0_0 and 1_1 transitions T must be 0 and for 0_1 and 1_0 transitions must be 1.

16. Define sequential circuit.

In sequential circuits the output variables dependent not only on the present input variables but they also depend up on the past history of these input variables.

17. Give the comparison between combinational circuits and sequential circuits.

Combinational circuits Sequential circuits Memory unit is not required Memory unity is

Required Parallel adder is a combinational circuit Serial adder is a sequential circuit.

18. What do you mean by present state?

The information stored in the memory elements at any given time define.s the present state of the sequential circuit.

19. What do you mean by next state?

The present state and the external inputs determine the outputs and the next state of the sequential circuit.

20. State the types of sequential circuits?

1. Synchronous sequential circuits 2. Asynchronous sequential circuits

21. Define synchronous sequential circuit

In synchronous sequential circuits, signals can affect the memory elements only at discrete instant of time.

22. Define Asynchronous sequential circuit?

In asynchronous sequential circuits change in input signals can affect memory element at any instant of time.

23. Give the comparison between synchronous & Asynchronous sequential circuits?

Synchronous sequential circuits Asynchronous sequential circuits. Memory elements are

locked flip-flops Memory elements are either unlocked flip - flops or time delay elements.

24. What is race around condition?

In the JK latch, the output is feedback to the input, and therefore changes in the output results change in the input. Due to this in the positive half of the clock pulse if J and K are both high then output toggles continuously. This condition is known as race around condition.

25. Give the comparison between synchronous & Asynchronous counters.

26. Asynchronous counters

- In this type of counter flip-flops are Connected in such a way that output of 1st Flip-flop drives the clock for the next Flipflop
- All the flip-flops are not clocked Simultaneously

Synchronous counters

- In this type there is no connection between output of first flip-flop and clock input of the next flip – flop
- All the flip-flops are clocked simultaneously

PART B

1. Explain the operation of a master slave JK flip flop **(8) (APRIL/MAY 2015) (MAY/JUNE 2016,17)**
2. Explain the realization of JK flip flop from T flip flop**. (7) (MAY 17)**
3. Explain the various types of triggering with suitable diagrams. Compare their merits and demerits **(8) (Nov/Dec 2014)**
4. Design BCD ripple counter using JK flip-flop **[16 Mark] [April/May 10]** [OR]
   - Design asynchronous BCD counter using JK flip-flop **[16 Mark] [May/June 14][April/May 11]**
5. Design an asynchronous BCD counter using JK flip flop **(16) (May/June 2011) & (May/June 2010) &(8)(May/June 2014)**
6. Design a 4-bit parallel-in serial-out shift register using D flip flops**. (7**) **(MAY 17)**
7. Design a 5 bit ring counter and mention its applications**.(6) (MAY 17)**
8. A sequential circuit with two D Flip-flops A and B, input X and output Y is specified by the following next state and output

   equations. $A(t+1) = AX + BX$, $B(t+1) = A'X$,$Y = (A+B)X'$ diagram.**[16 Mark][May/June 2012]**
9. Write short notes on SIPO and draw the output waveforms. **(6)(MAY 17)**
10. A sequential circuit with D flip flops A and B, input X and output Y is specified by the following next state and output equations
    A(t+1) = AX + BX,
    B(t+1) = A'X
    Y = (A+B)X'
    Draw the logic diagram, derive state table and state diagram. **(12) (NOV/DEC 2015)**
11. Sketch the state diagram and state table for 'D' and 'JK' flip-flops? **[6 Mark] [Nov/Dec 2012]**

UNIT-IV

ASYNCHRONOUS SEQUENTIAL CIRCUITS AND PROGRAMMABLE LOGIC DEVICES

1. **What is ROM?**

   A read only memory (ROM) is a device that includes both the decoder and the OR gates

   within a single IC package. It consists of n input lines and m output lines. Each bit Combination of the input variables is called an address. Each bit combination that comes out of the output lines is called a word. The number of distinct addresses possible with n input variables is 2n.

2. **What are the types of ROM?**

   1. PROM 2. EPROM 3. EEPROM

3. **What is PROM?**

   PROM (Programmable Read Only Memory) it allows user to store data or program. PROMs use the fuses with materiallike nichrome and polycrystalline. The user can blow these

   fuses by passing around 20 to 50 mA of current for the period 5 to 20μs.The blowing of fuses is called programming of ROM. The PROMs are one time programmable. Once programmed, the information is stored permanent.

4. **What is EPROM?**

   EPROM (Erasable Programmable Read Only Memory) EPROM use MOS circuitry. They store 1's and 0's as a packet of charge in a buried layer of the IC chip. We can erase the stored data in the EPROMs by exposing the chip to ultraviolet light via its quartz window for 15 to 20 minutes. It is not possible to erase selective information. The chip can be reprogrammed.

5. **What is EEPROM?**

   EEPROM (Electrically Erasable Programmable Read Only Memory). EEPROM also use

   MOS circuitry. Data is stored as charge or no charge on an insulated layer or an insulated floating gate in the device. EEPROM allows selective erasing at the register level rather than erasing all the information since the information can be changed by using electrical signals.

6. **Define address and word:**

   In a ROM, each bit combination of the input variable is called on address. Each bit combination that comes out of the output lines is called a word.

7. **What are the types of ROM.?**

1. Masked ROM. 2. Programmable Read only Memory
Erasable Programmable Read only memory.

Electrically Erasable Programmable Read only Memory.

8. **What is mask - programmable?**

With a mask programmable PLA, the user must submit a PLA program table to the manufacturer.

9. **What is field programmable logic array?**

The second type of PLA is called a field programmable logic array. The user by means of certain recommended procedures can program the EPLA.

10. **List the major differences between PLA and PAL**

PLA: Both AND and OR arrays are programmable and Complex Costlier than PAL

PAL:AND arrays are programmable OR arrays are fixed Cheaper and Simpler

11. **Define PLD.**

Programmable Logic Devices consist of a large array of AND gates and OR gates that Can be programmed to achieve specific logic functions.

12. **Give the classification of PLDs.**

PLDs are classified as PROM (Programmable Read Only Memory), Programmable Logic Array (PLA), Programmable Array Logic (PAL), and Generic Array Logic (GAL)

13. **Define PROM.**

PROM is Programmable Read Only Memory. It consists of a set of fixed AND gates Connected to a decoder and a programmable OR array.

14. **Define PLA.**

PLA is Programmable Logic Array (PLA). The PLA is a PLD that consists of a Programmable AND array and a programmable OR array.

15. **Define PAL.**

PAL is Programmable Array Logic. PAL consists of a programmable AND array and a fixed OR array with output logic.

16. **Why the input variables to a PAL are buffered**

The input variables to a PAL are buffered to prevent loading by the large number of AND gate inputs to which available or its complement can be connected.

17. **What is CPLD?**

CPLDs are Complex Programmable Logic Devices. They are larger versions of PLDs with a centralized internal interconnect matrix used to connect the device macro cells together

18. **Define RAM.**

RAM is Random Access Memory. It is a random access read/write memory. The data can be read or written into from any selected address in any sequence.

19. **Define Static RAM and dynamic RAM.**

Static RAM use flip flops as storage elements and therefore store data indefinitely as long as dc power is applied. Dynamic RAMs use capacitors as storage elements and cannot retain data very long without capacitors being recharged by a process called refreshing.

20. **List the two types of SRAM.**
Asynchronous SRAMs and Synhronous Burst SRAMs

21. **List the basic types of DRAMs.**

Fast Page Mode DRAM,Extended Data Out DRAM(EDO DRAM),Burst EDO DRAM and Synchronous DRAM.

22. **What are Flash memories?**

They are high density read/write memories that are non-volatile, which means data can be stored indefinitely with out power.

23. **What is a FIFO memory?**

The term FIFO refers to the basic operation of this type of memory in which the first data bit written into the memory is to first to be read out.

PART B

1. Sketch the transition table and state table for an asynchronous sequential circuit described by the following Boolean expressions:$Y_1 = xy_1 + x'y_2, Y_2 = xy_1' + x'y_2$.**[8 Mark][Nov/Dec 2012]**
2. For the given Boolean function obtain the hazard-free circuit F(*A,B,C,D*)=$\sum m(1,3,6,7,13,15)$ (8) **(APRIL/MAY 2015)**
3. Implement the following logic and analyze for the pressure of any hazard $f=x_1x_2+x_1'x_3$. If hazard is present briefly explain the type of hazard and design a hazard-free circuit. (7)
   Implement the following functions using programmable logic array:
   $F_1(x,y,z)=\Sigma m(0,1,3,5,7)$
   $F_2(x,y,z)=\Sigma m(2,4,6)$ **(6) (MAY 2017)**
4. Illustrate the analysis procedure of Asynchronous Sequential circuit with an example**.[16 Mark] [May/June 2013][May/June 2012] [Nov/Dec 2010]**
5. Implement the following functions using PLA:

   $F_1 = \sum m(1,2,4,6);\ F_2 = \sum m(0,1,6,7);\ F_3 = \sum m(2,6)$.**[8 Mark][Nov/Dec 2013]**

6. Design BCD to Excess 3 code converter using PAL.**[8 Mark]**
7. A combinational logic circuit is defined by the following function

$f_1(a,b,c) = \sum(0,1,6,7)$; $f_2(a,b,c) = \sum(2,3,5,7)$. Implement the circuit with a PAL having three inputs, three product terms and two outputs.**[10 Mark] [May/June 2012]**

8. Implement the following function using PLA and PAL: f(*x,y,z*) = Σm(0,1,3,5,7) **(10) (MAY 2016)**
9. Generate the following Boolean functions with a PAL with 4 inputs and 4 outputs Y_3 = A'BC'D + A'BCD' + ABC'D, Y_2 = A'BCD' + A'BCD + ABCD, Y_1 = A'BC' + A'BC + AB'C + ABC', Y0 = ABCD.**[8 Mark][Nov/Dec 08]**

UNIT-V

VHDL

1. What is Verilog?

Verilog is a general purpose hardware descriptor language. It is similar in syntax to the C programming language. It can be used to model a digital system at many levels of abstraction anging from the algorithmic level to the switch level.

2. What are the various modeling used in Verilog?

1. Gate-level modeling 2. Data-flow modeling

3. Switch-level modeling 4. Behavioral modeling

3. What is the structural gate-level modeling?

Structural modeling describes a digital logic networks in terms of the components that wake up the system. Gate-level modeling is based on using primitive logic gates and specifying how they are wired together.

4. What is Switch-level modeling?

Verilog allows switch-level modeling that is based on the behavior of MOSFETs. Digital circuits at the MOS-transistor level are described using the MOSFET switches.

5. What are identifiers?

Identifiers are names of modules, variables and other objects that we can reference in the design. Identifiers consists of upper and lower case letters, digits 0 through 9, the underscore character(_) and the dollar sign($). It must be a single group of characters. Examples: A014, a, b, in_o, s_out

6. What are the value sets in Verilog?

Verilog supports four levels for the values needed to describe hardware referred to as value sets.

Value levels Condition in hardware circuits

- x 0 Logic zero, false condition

- 1 Logic one, true condition
- X Unknown logic value
- Z High impedance, floating state

7. What are the types of gate arrays in ASIC?

1) Channeled gate arrays 2) Channel less gate arrays 3) Structured gate arrays

8. Give the classifications of timing control

Methods of timing control:

1. Delay-based timing control 2. Event-based timing control

3. Level-sensitive timing control

Types of delay-based timing control:

1. Regular delay control 2. Intra-assignment delay control
3. Zero delay control

Types of event-based timing control:

1. Regular event control 2. Named event control
3. Event OR control 4. Level-sensitive timing control

9 .Give the different arithmetic operators?

Operator symbol Operation performed Number of operands

* Multiply Two
/ Divide Two +
Add Two

- Subtract Two
% Modulus Two

** Power (exponent) Two

10. What are gate primitives?

Verilog supports basic logic gates as predefined primitives. Primitive logic function keyword provides the basics for structural modeling at gate level. These primitives are instantiated like modules except that they are predefined in verilog and do not need a module definition. The important operations are and, nand, or, xor, xnor, and buf(non-inverting drive buffer).

12. Give the two blocks in behavioral modeling.

1. An initial block executes once in the simulation and is used to set up initial conditions and step-by-step data flow.

2. An always block executes in a loop and repeats during the simulation.

13. What are the types of conditional statements?

1. No else statement

Syntax: if ([expression]) true – statement;

2. One else statement

Syntax: if ([expression]) true – statement;

else false-statement;

3. Nested if-else-if

Syntax : if ([expression1]) true statement 1;

else if ([expression2]) true-statement 2;

else if ([expression3]) true-statement 3;

else default-statement;

14.What Is HDL?

CAD tools areused in the design of digital systems.one such tool is Hardware Description Language

15.What are the main components of VHDL?

- Package
- Entity
- Architecture
- Configuration

PART B

1. Write HDL program for Full Adder **.[8 Mark][Apr/May 2010]**
2. Write a VHDL code to realize full adder using both behavioural and structural modelling **(16) (APRIL/MAY 2015)&(Nov/Dec 2014)**
   - Explain the concept of behavioural and structural modeling in VHDL. Take the example of Full Adder design for both and write the coding **(16) (Nov/Dec 2014)**
   - Write the VHDL code to realize a decade counter with behavioural modeling**(8) (MAY/JUNE 2016)**
   - Write a VHDL program for Full adder using structural modeling.**(8) (NOV/DEC 2015)**
   - Explain the concept of structural modeling in VHDL with an example of full adder.**(13)[NOV 16]**
3. Write an HDL behavioral description of JK flip-flop using if-else statement based on the value of present state? **[8 Mark][Apr/May 2010]**
4. Write the VHDL code for Mod-6 Counter? **[16 Mark][May/June 2012] [Apr/May 2011]**
5. Write the VHDL code to realize a 3- bit gray code counter using case statements **(16) (APRIL/MAY 2015)**
6. Design a 4*4 array multiplier and write the VHDL code to realize it using structural modeling. **(13)[MAY 2017]**
7. Design a 3-bit magnitude comparator and write the VHDL code to realize it using structural modeling. **[13] [MAY 2017]**
8. Explain the various operators supported by VHDL. **(8) (MAY/JUNE 2016)**
9. Briefly discuss the use of 'Packages' in VHDL? **[8 Mark] [Nov/Dec 2012]**
10. Explain functions and subprograms with suitable examples. **(8)(MAY/JUNE 2016)**